



# SMT Area Array Package Turns 30 Years Old!

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The first area array packages was assembled and tested some 30 years ago in a joint industry research packaging lab in Austin Texas under the direction principal researcher Steve Stach. Two types of new SMT array packages were modified from standard thru-hole pin grid array (PGA) package. The first group consisted of pin grid arrays with thin and thick leads cut short and surface mounted directly to surface pads. The second group of parts were pin grid arrays without pins attached, dubbed pad grid arrays.

Both groups were soldered to test boards and were subjected to a series of test including air-to-air thermal cycling from -65C to+125C, power cycling from ambient to 125C, and flex testing on a mandrel with a 40" radius until failure.

Both infrared and vapor phase solder reflow methods were used to attach the SMT test arrays. A rework cycle was also included in the process evaluation for selected parts.

Test results confirmed that the surface mount array package was a viable alternative to the quad flat pack (QFP) which had reached its I/O limit at around 256. SMT array packages could in theory go to I/O counts beyond 1,000. Data confirmed that pad grid arrays were not as survivable as leaded and more compliant pin grid cousins. The following chart (55) shows the effect of lengthening the pins in the thermal cycle test.

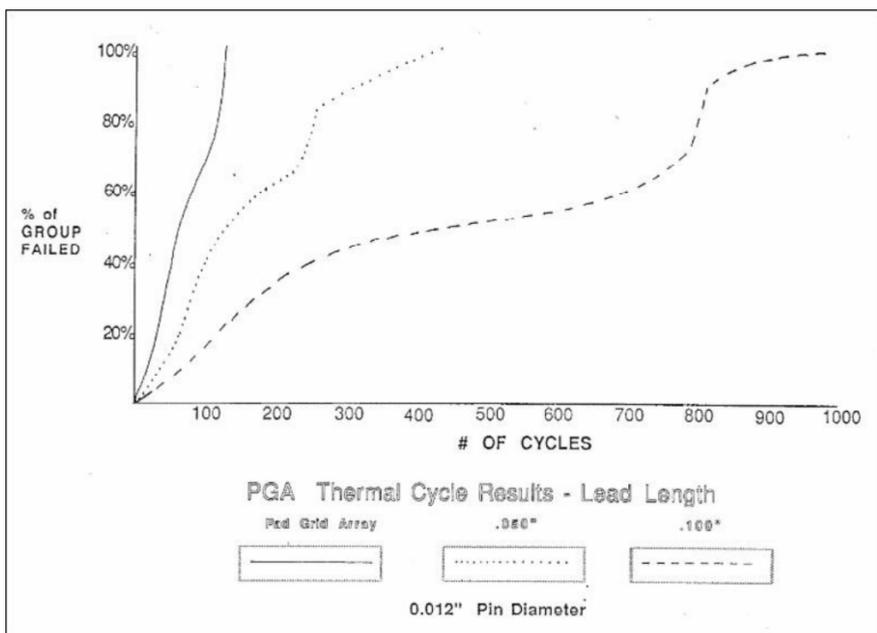
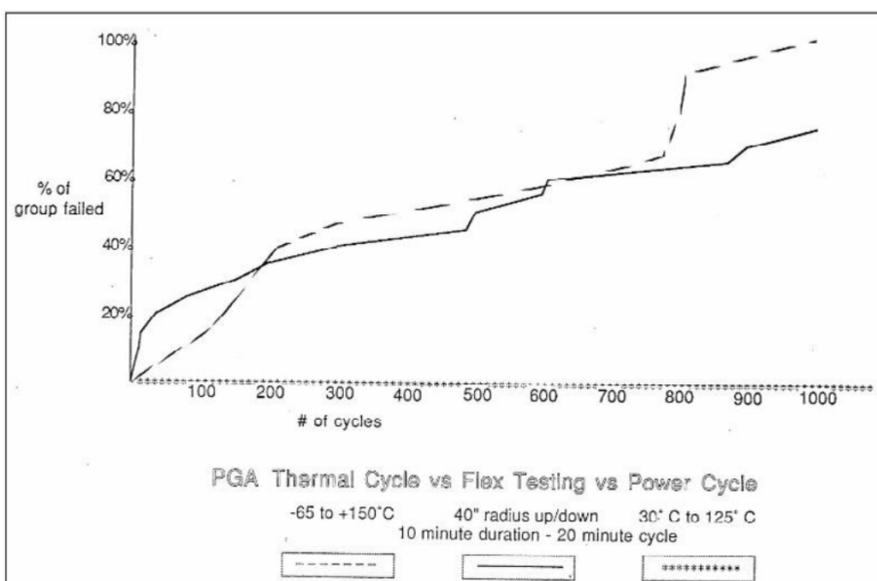


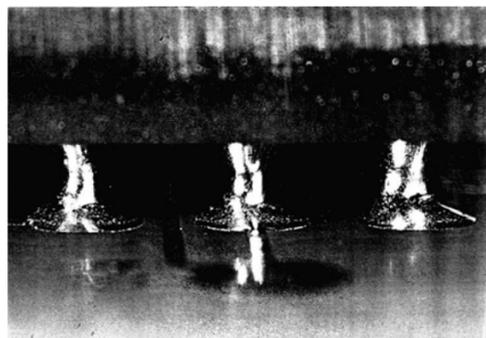
Chart showing the relationship of lead length and electro-mechanical survivability Mr. Stach recalled "The early failure of the leadless pad grid arrays indicated that array packages for this type must either be small flip chip style packages or have large robust pads much like the QFN's of today." He went on to say "The leaded SMT arrays were more reliable when stressed and pointed package designers towards mechanically compliant structures such as ball grid arrays and column grid arrays."

There was a significant difference when the packages were evaluated in electrical power cycling the package from 30C to 125C while the test board remained unheated. The power cycle samples had no failure after 800 cycles. Only leaded samples were tested. The results are shown in chart below

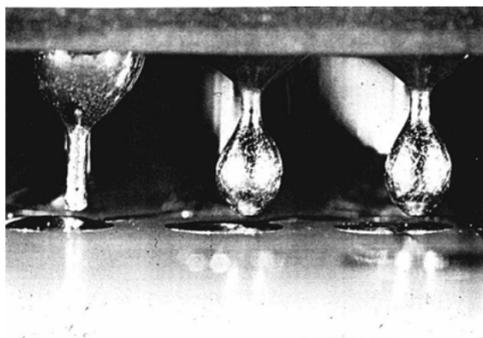


### PGA Thermal vs Power vs Flex Cycle

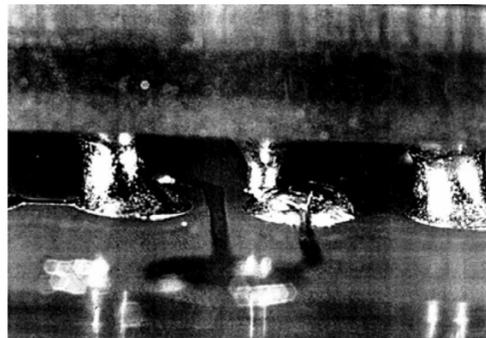
Process problems were encountered including solderability, bent pins from handling, and pin to pad alignment. On a positive note, the pad to pad samples were found to be self-aligning, correcting even when misplaced up to 50%. There were no real differences noted in the reliability resulting from the solder reflow method used. The study also showed that the array packages could be reworked with traditional hot gas rework stations.



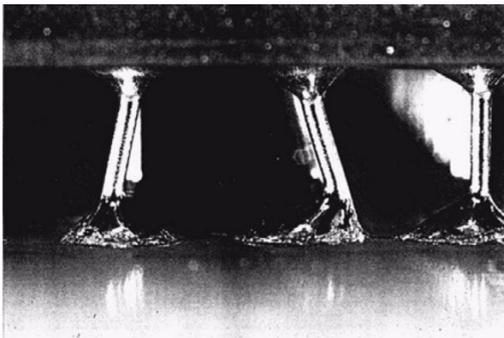
poor solder connection



wick open



misaligned pga



bent pins

From its humble beginnings, the SMT area array package has become the go to standard for both high I/O and high energy packages in a short 30 years. It is found today on virtually every electronic assembly manufactured today and will most likely hold that position for many more years to come.

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